Purdue University
Purdue e-Pubs

ECE Technical Reports | Electrical and Computer Engineering

2-2-2006

Optimization of Surface Orientation for High-Performance, Low-Power and Robust FinFET SRAM

Saakshi Gangwal
Purdue University

Saibal Mukhopadhyay
Purdue University

Kaushik Roy
Purdue University

Follow this and additional works at: http://docs.lib.purdue.edu/ecetr

Gangwal, Saakshi; Mukhopadhyay, Saibal; and Roy, Kaushik, "Optimization of Surface Orientation for High-Performance, Low-Power and Robust FinFET SRAM" (2006). *ECE Technical Reports.* Paper 330.
http://docs.lib.purdue.edu/ecetr/330

This document has been made available through Purdue e-Pubs, a service of the Purdue University Libraries. Please contact epubs@purdue.edu for additional information.

Optimization of Surface Orientation for High-Performance, Low-Power and Robust FinFET SRAM

By

Saakshi Gangwal,
Saibal Mukhopadhyay,
and
Kaushik Roy

Dept. of Electrical and Computer Engineering,
Purdue University
West Lafayette, IN-47907, USA

This work is supported in part by GSRC, SRC, Intel, IBM and Freescale Corp.

Abstract

We analyze the impact of surface orientation on stability and performance of FinFET SRAMs. We show that devices with proper orientations can improve static noise margin (SNM, 23-35%) and access time (22-33%) of 32nm FinFET SRAM compared to a design with devices of single (110) orientation.

Introduction

Mobility of PMOS and NMOS devices can be improved by optimizing orientation of crystal surface, resulting in better circuit performance [1]. For multiple-gate vertical devices, such as FinFETs, surface orientation can be changed by modifying the layout of the devices (Fig. 1). This suggests that, orientation optimization can enhance the performance of FinFET logic circuits [1]. However, the effect of crystal orientation on FinFET SRAM has not been analyzed. In this paper, for the first time, we analyze the effect of surface orientation on FinFET SRAM in sub-50nm technologies. Using mixed-mode device simulations [2] with calibrated mobility values [1], we show that, orientation optimization and design of multi-orientation FinFET SRAM improve cell stability and performance. It is observed that, considerable improvement in static noise margin (SNM) and cell access time (AT) is achievable with optimized multi-orientation SRAM compared to the cell designed with all (110) (default orientation for FinFET devices on (100) wafer) devices.

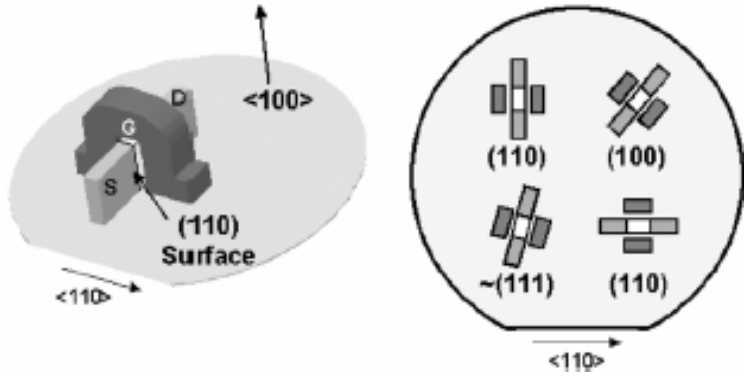


Fig. 1: Modification of surface orientation in FinFET

Effects of Surface Orientation in FinFET Devices

We studied SRAM designed with 32nm FinFET devices (Tsi=7nm, EOT=1.73nm with oxynitride, H_{FIN}=36nm, V_{DD}=0.8) using mixed-mode device simulations [2]. The electron and hole mobilities for different orientations are first calibrated against the measured data obtained from [3]. Maximum mobility for NMOS is along (100) whereas that for PMOS is along (110) (Fig. 2). Due to velocity saturation, the change in current is lower than the change in mobility [1]. Due to the differences in interface trap density, oxide charge and quantum mechanical effects (different electron/hole effective mass for three orientations), there can be a marginal shift (~15-20mV) in device Vt along different orientations [1, 3], resulting in a nominal change in the subthreshold leakage. We have not considered these effects in our simulation. This is justified for short channel devices as discussed in [1]. The surface orientation is shown to have negligible impact on gate leakage. Hence, in this study we primarily investigated surface orientation effect on linear and saturation current, which impact the

stability and performance of an SRAM cell.

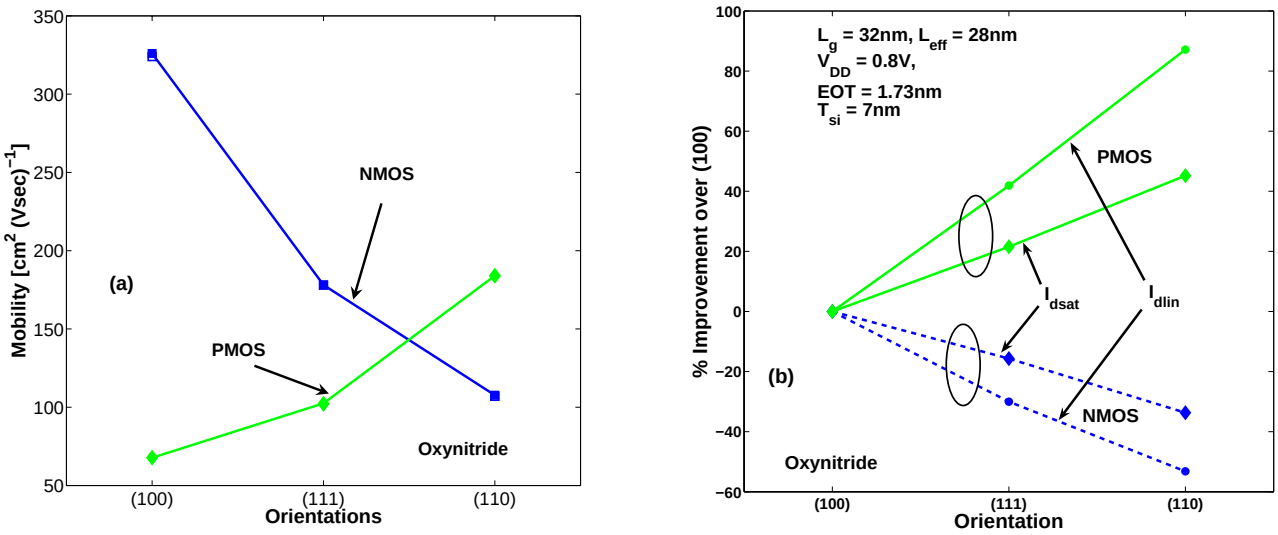


Fig. 2: Effect of surface orientation on (a) Mobility (b) Current.

Optimization of Surface Orientation for FinFET SRAM

The β-ratio between different transistors of an SRAM cell is critical to its stability. In planar technologies (bulk-CMOS) sizes of different transistors are used to optimize β-ratio [4]. However, in FinFET SRAM, sizing opportunities are limited as device widths are quantized (in quanta of fin height). Hence, modification of device mobility with fin orientation can be used to optimize β-ratio in FinFET SRAM. In this analysis, we considered a cell designed with all single fin devices.

Read Stability: A higher mobility of pull-down (PD) NMOS and a lower mobility of access (AX) NMOS helps reduce the read voltage (V_{READ}, voltage to which node storing "0" rises while reading). Lowest

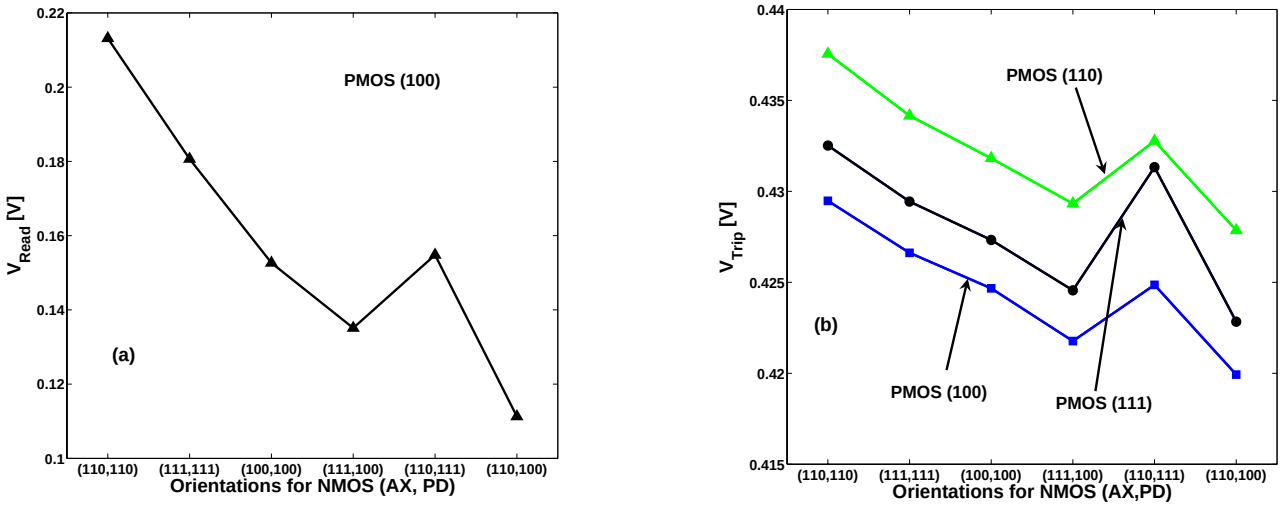


Fig. 3: Effect of orientation on (a) Read Voltage, (b) Trip-Point

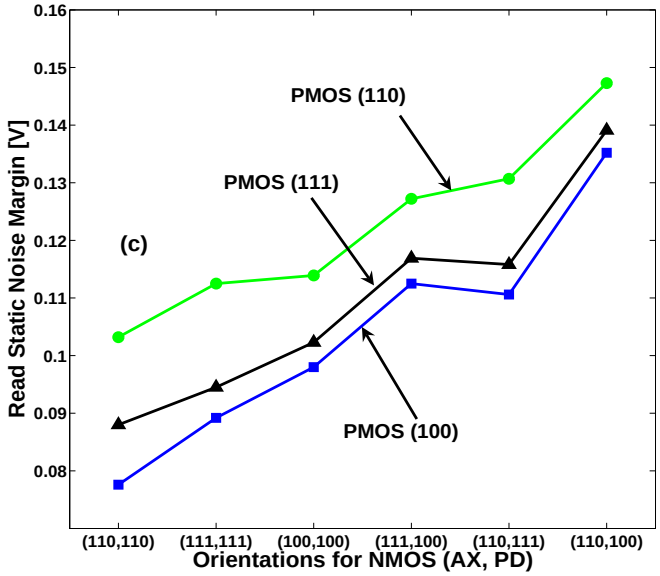


Fig. 3: Effect of orientation on (c) Read SNM

V_{READ} can be achieved with (110) AX and (100) PD devices (Fig. 3a). Since linear current depends more strongly on orientation compared to the saturation current (Fig 2b), V_{READ} for (110) PD & (110) AX is higher than that for (100) PD & (100) AX (Fig. 3a). On the other hand, higher mobility of PMOS pull-up (PUP) compared to PD increases the trip-point of the inverter associated with the node storing "1" (V_{TRIPRD}) (Fig. 3b). Since read stability depends on (V_{TRIPRD}- V_{READ}) it was observed that, maximum read stability, represented by maximum SNM, is obtained for (110) PUP, (100) PD and (110) AX (43% larger from all (110) devices, Fig. 3c).

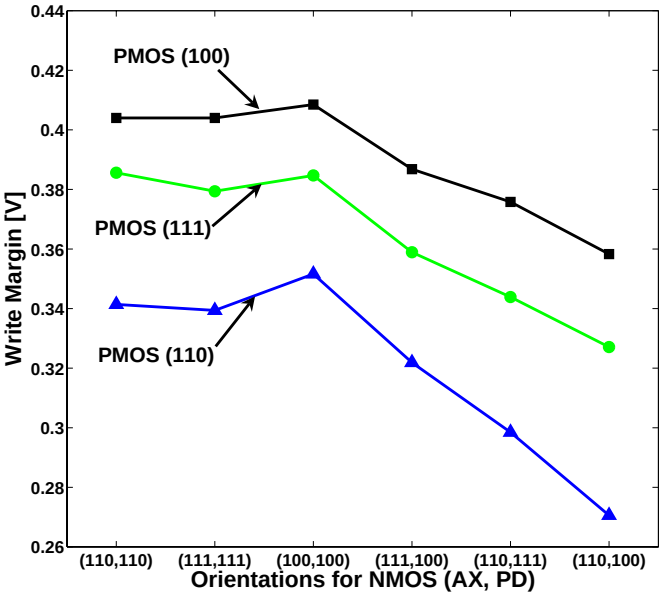


Fig. 4: Write Margin

Write Stability: Use of a weaker PUP and stronger AX helps the node storing "1" to discharge faster [4]. A stronger PUP and weaker PD increases trip-point of the inverter associated with the node storing

"0" and helps the write operation. Due to these effects we observed that, the cells with all (100) devices have maximum write margin (WM, the maximum voltage on a bitline that allows writing to the cell while the other bit-line is at V_{DD}) -- 16% higher than all (110) (Fig. 4).

Hold Stability: Hold stability of the cell is measured using the hold SNM. Use of (110) PUP and (100) PD devices (node storing '1' & '0' are strongly coupled to V_{DD} & V_{SS}) improves the hold SNM. However, fin orientations were found to have a weak impact on hold SNM (Fig. 5).

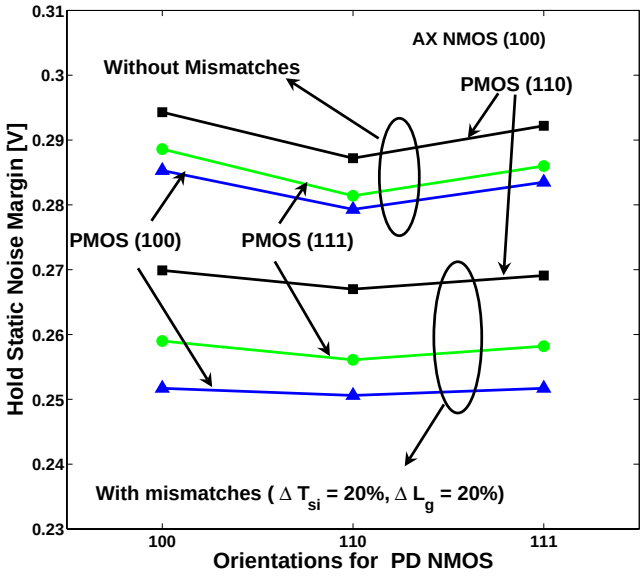


Fig. 5: Hold Stability

Access Time: Fin orientations of AX and PD impact the read current and hence the Access time of the cell (Fig. 6). The access time was found to be minimum for (100) AX & (100) PD (~38% higher than all (110)).

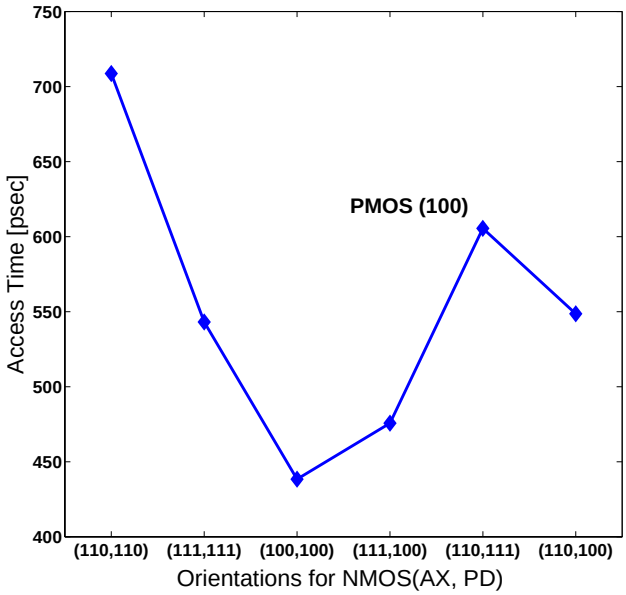


Fig. 6: Access Time

Due to conflicting requirements for write and read stabilities (e.g. orientation required for maximum SNM has a poor WM, Fig. 3, 4) proper optimization of different fin orientations is required to improve cell stability. Fig. 7 shows a set of multi-oriented cells that can achieve significant improvement in read SNM (23-35%) and access time (22-33%) compared to conventional design with all (110) devices.

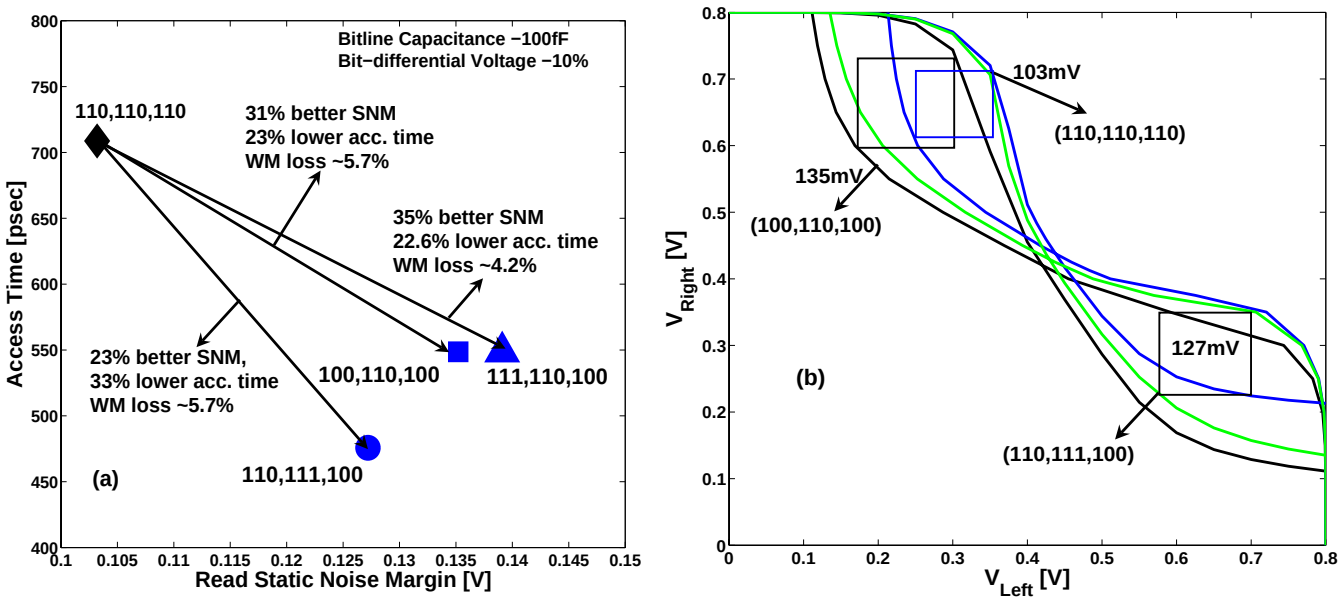


Fig. 7: Optimized multi-oriented cells: (a) Access Time vs Read SNM, (b) Butterfly Curves

It is also observed, that the optimized fin-orientations have a marginal impact on WM and hold SNM (Fig. 7). However, for FinFET SRAM designed on (100) wafer, orientations other than (110) require a rotated (~45^0 for (100), ~35^0 for (111)) layout.

Table-I: Area penalty compared to **all (110) cell**		
PUP,AX,PD	Wafer (100)	Wafer (110)
(110),(111),(100)	8.4%	10.43%
(100),(110),(100)	21.96%	14.1%
(111),(110),(100)	22.3%	16.4%

The layout of the multi-oriented cells (using the guideline shown in [5]) shows that, the use of rotated devices requires a larger cell area as compared to all (110) devices case (Fig. 8, Table-I). It can be observed that (110) PUP, (111) AX and (100) PD configuration gives significant improvement in cell stability (~23% better read SNM) and performance (~33% lower AT) with minimum area penalty (~8%, Fig. 7 & Table-I). If (110) wafer is used, since (110) and (100) orientations require a 90^0

rotation, the area penalty associated with multi-oriented cells can be lower (Table-1, Fig. 8). With (110) wafer, (100) PUP, (110) AX and (100) PD orientation could be better compared the other ones in Fig. 7 as this combination of device orientations gives better SNM, higher WM while taking only a marginally higher area. Moreover, it also does not require rotated device layout ('Manhattan geometry', Fig. 8).

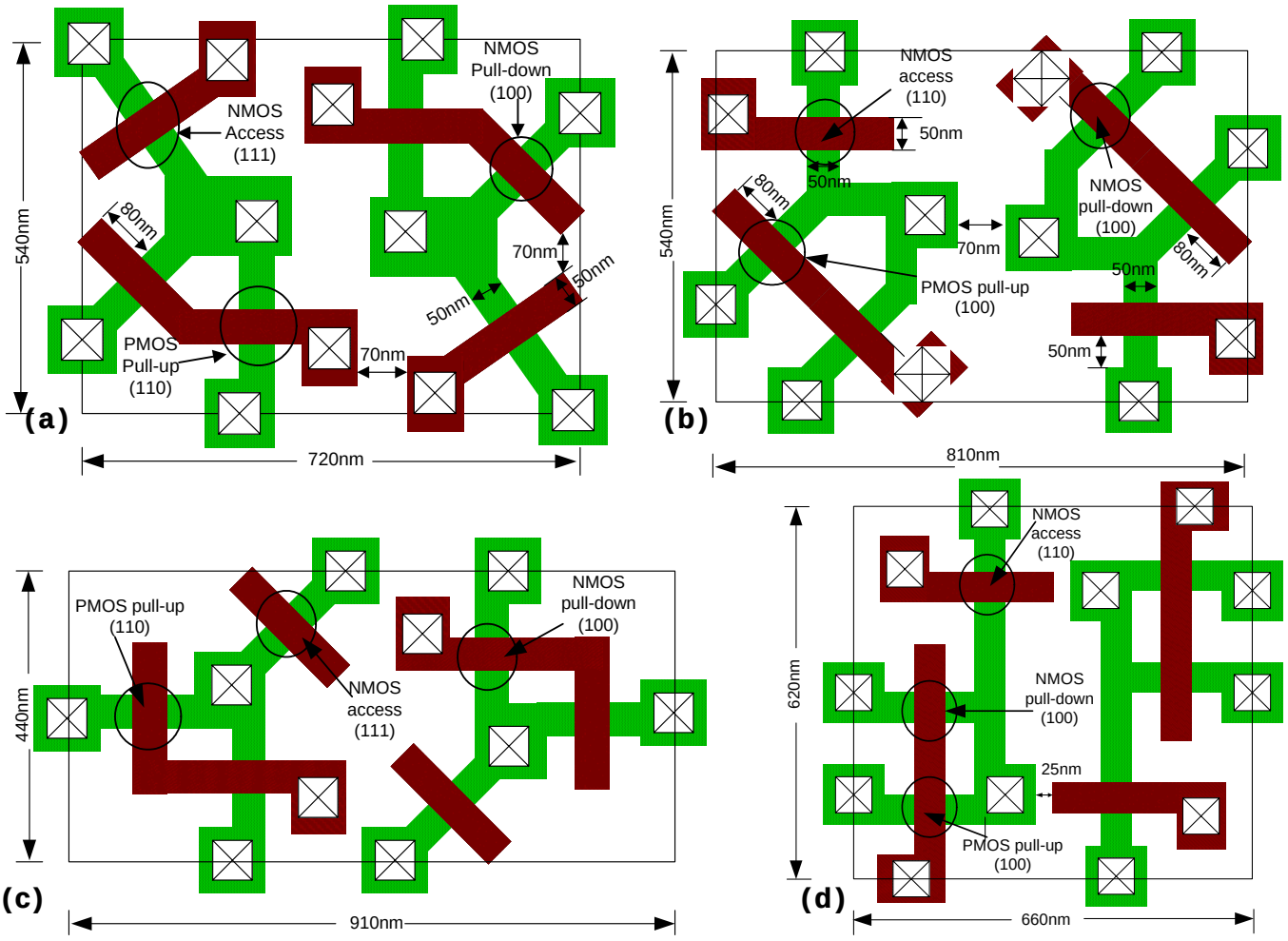


Fig. 8: Multi-orientation layouts: (110) PUP, (111) AX, (100) PD in (a) wafer (100), (c) wafer (110). (100) PUP, (110) AX, (100) PD in (b) wafer (100), (d) wafer (110).

Simulations considering worst-case device mismatches (20% change Tsi and Lgate) show that multi-oriented cells have lower degradation in read SNM, WM and hold SNM due to process variation (Fig. 5, 9). Hence, optimization of fin orientation can improve the cell robustness under process variation. However, printing rotated device may result in additional sources of process variation, which has not been considered in this analysis.

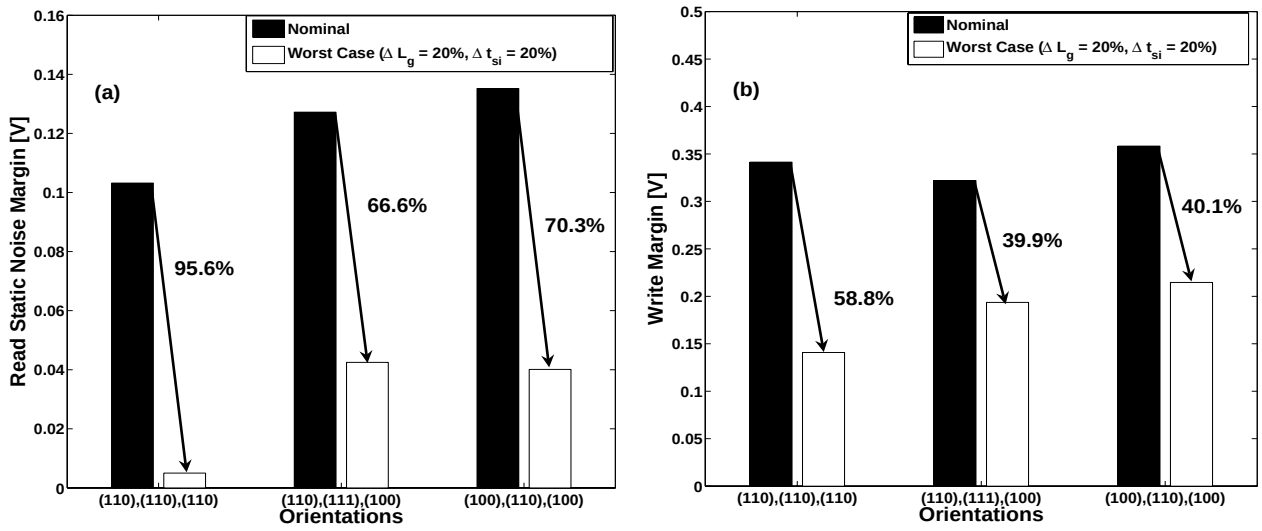


Fig. 9: (a) Read SNM (b)Write Margin with process variations.

The stability of an SRAM cell can also be improved by optimizing the number of fins for different devices. For example, use of 2-fin PD improves the read SNM for all (110) cell (by~55%) but reduces WM (~37%). We observed that, with multi-oriented single-fin cells of comparable area we can achieve a better WM (~50-67%) and Access Time compared to the 2-fin PD cell with a nominal SNM degradation (Fig. 11). This suggests that multi-orientation can be effectively used to optimize the performance and stability of FinFET SRAM design.

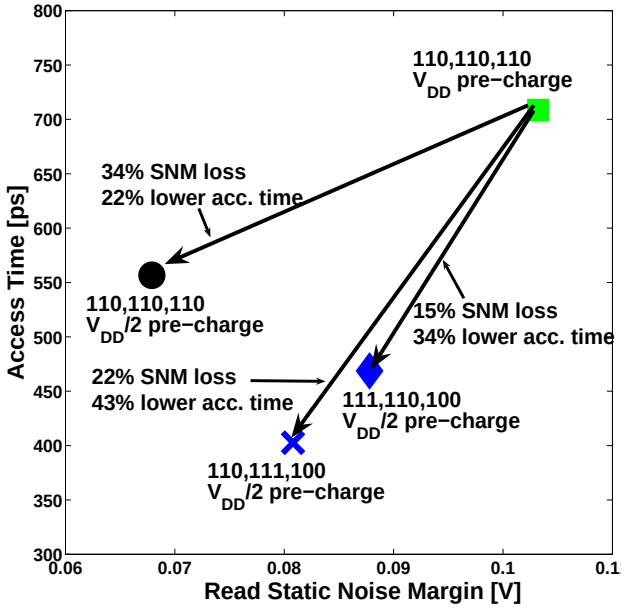


Fig. 11: Effect of fin orientation on $V_{DD}/2$ precharge SRAM. Multi-oriented cell improve the feasibility of $V_{DD}/2$ precharge.

Optimization of fin orientation also improves the feasibility of $V_{DD}/2$ bitline precharge scheme in SRAM. Apart from reducing the bitline leakage, $V_{DD}/2$ bitline precharge can also increase the bit-differential since the two bit-line voltages move in opposite direction while reading and thus resulting in a better performance. The principal issue with this scheme is a large degradation in read SNM as the node storing "1" reduces from V_{DD} (34% SNM degradation for all (110) cell). With a multi-oriented SRAM having lower AX to PD mobility ratio the SNM loss in $V_{DD}/2$ precharge scheme can be significantly reduced (~15%, Fig. 10)

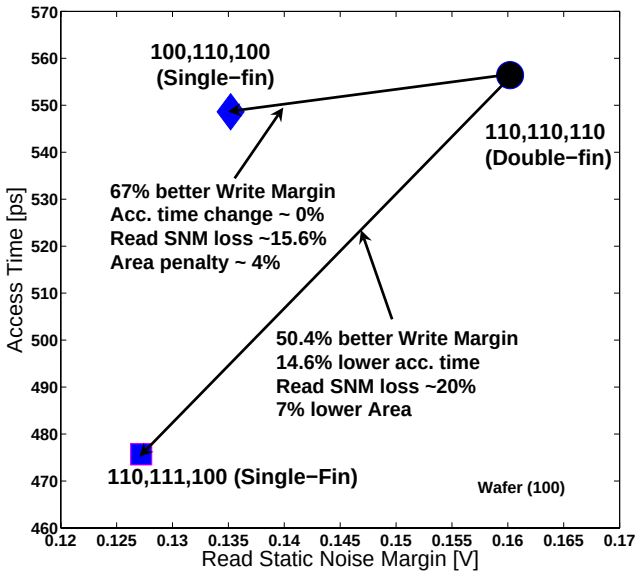


Fig. 10: Comparison of multi-oriented single fin cells with all (110) 2 fin PD cell.

Conclusions

A detailed analysis of crystal orientation on the leakage, performance and stability of FinFET SRAM cell is presented. Our analysis shows that SRAM designed with optimized fin-orientation can improve cell stability and performance. Hence, we believe that multi-oriented FinFETs are suitable options for high-performance and stable SRAMs in sub-50nm technology.

REFERENCE

[1] L. Chang, et. al. IEEE TED, pp. 1621-27, Oct. 2004.

[2] MEDICI Version V-2003.12-0, Synopsys.

[3] M. Yang, et. al. IEEE EDL , pp. 339-41, May 2003.

[4] J. Rabaey, et. al., *Digital Integrated Circuits*, Prentice Hall, 2002.

[5] Z. Guo, et. al., ISLPED, 2005.